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APPLICANTS:	Shepard		
SERIAL NO.:	08/863,156 Application for Reissue of U.S. Patent No. 5,889,694	GROUP NO.:	2818
FILING DATE:	May 27, 1997	EXAMINER:	Andrew Q. Tran
TITLE:	DUAL-ADDRESSED RECTIFIER STORAGE DEVICE		

PRELIMINARY AMENDMENT

Box REISSUE
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Preliminary Amendment accompanies the filing of the subject reissue application. Applicant believes that the check submitted with this filing is sufficient to cover the fees due as a result of entering this amendment, however in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Attorney's Deposit Account No. 20-0531.

In the Claims

Please cancel claims 1-3, 14-17, 20 and 25-27, and amend the remaining claims as follows:

4. (Amended) The [digital logic device of claim 1, wherein one of said plurality of generally parallel conductive means] circuit of claim 31, wherein one of the sets of conductive address lines is a plurality of generally parallel doped regions within a semiconductor material.

5. (Amended) The [digital logic device of claim 1, wherein one of said plurality of generally parallel conductive means]circuit of claim 31, wherein one of the sets of conductive address lines is a plurality of generally parallel metalized regions.

6. (Amended) The [digital logic device of claim 1]circuit of claim 31, wherein said addressing [means] circuitry comprises [means]circuitry to sequentially select [addressed]storage locations.

7. (Amended) The [digital logic device of claim 1]circuit of claim 31, wherein said addressing [means]circuitry comprises [means]circuitry to randomly select [addressed]storage locations.

8. (Amended) The [digital logic device of claim1]circuit of claim 31, further comprising display means for displaying alphanumeric or graphic information to [its]a user.

9. (Amended) The [digital logic device of claim 1]circuit of claim 31, further comprising input means to enable its user to alter its operation.

10. (Amended) The [digital logic device of claim 1]circuit of claim 31, wherein part or all of said [one more electronic storage means are]circuit is removable or replaceable.

11. (Amended) The [digital logic device of claim 1]circuit of claim 31, wherein output from the [device]circuit is in a digital format.

12. (Amended) The [digital logic device of claim 1]circuit of claim 31, wherein output from the [device]circuit is in an analog format.

13. (Amended) The [digital logic device of claim 1]circuit of claim 31, wherein output from the [device]circuit is in either a digital format or an analog format.

18. (Amended) The [storage device of claim 17]circuit of claim 5, wherein said [rectifying conductive means between said plurality of generally parallel doped regions and a plurality of generally parallel metalized regions]nonlinear elements [is]are of the metal-on-semiconductor junction type.

19. (Amended) The [storage device of claim 17]circuit of claim 5, wherein said [rectifying conductive means between said plurality of generally parallel doped regions and a plurality of generally parallel metalized regions]nonlinear elements [is]are of the p-n junction type.

21. (Amended) The [storage device of claim 14]circuit of claim 31, wherein said [rectifying conductive means is]nonlinear elements are comprised by a transistor as the base-emitter junction.

22. (Amended) The [storage device of claim 14]circuit of claim 31, further comprising means for retaining the address of the information to be accessed.

23. (Amended) The [storage device]circuit of claim 22, further comprising means for incrementing the retained address.

24. (Amended) The [storage device]circuit of claim 22, further comprising means for setting the retained address.

Please add the following new claims:

31. (New) An information-storage circuit, the circuit comprising:

a. first and second sets of conductive address lines overlapping with each other and defining storage locations at overlap regions;

b. a series of information-defining nonlinear elements bridging the address lines at least at some of the overlap regions, presence or absence of a nonlinear element at a storage location defining a bit state at the location; and

c. address circuitry for disabling all but a selected one of the first set of address lines.

32. (New) The circuit of claim 31 further comprising sensing circuitry for sensing the presence or absence of a nonlinear information-defining element bridging the selected first-set address line and at least a selected one of the second set of address lines to thereby determine the bit state at each storage location defined by selected address lines.

33. (New) The circuit of claim 31 wherein the all but one of the first set of address lines is disabled by shifting a voltage thereon.

34. (New) The circuit of claim 31 further comprising additional address circuitry for disabling all but a selected one of the second set of address lines.

35. (New) The circuit of claim 34 wherein the all but one of the second set of address lines is disabled by shifting a voltage thereon.

36. (New) The circuit of claim 34 wherein:

a. the information-defining nonlinear elements have a threshold activation voltage associated therewith;

b. the address circuitry comprises circuitry for setting all but the selected one of the first set of address lines to a first voltage level; and

c. the additional address circuitry comprises circuitry for setting all but the selected one of the second set of address lines to a second voltage level, the first and second voltage levels differing by at least the threshold activation voltage.

37. (New) The circuit of claim 36 wherein:

a. the address circuitry further comprises a first set of selectable disabling lines fewer in number than and connected to the first set of address lines by a first pattern of nonlinear elements, and circuitry for applying a third voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of address lines; and

b. the additional address circuitry further comprises a second set of selectable disabling lines fewer in number than and connected to the second set of address lines by a second pattern of nonlinear elements, and circuitry for applying a fourth voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of address lines.

38. (New) The circuit of claim 37 wherein the third voltage is substantially equal to the second voltage and the fourth voltage is substantially equal to the first voltage.

39. (New) The circuit of claim 38 wherein all of the nonlinear elements have a threshold activation voltage associated therewith, application of the threshold activation voltage across the nonlinear elements allowing current to flow therethrough.

40. (New) The circuit of claim 36 wherein the information-defining nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop so that an information-defining rectifier, if present at the storage location defined by the selected address lines, is forward biased.

41. (New) The circuit of claim 39 wherein all of the nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop.

42. (New) The circuit of claim 36 wherein the second voltage is ground or near to ground.

43. (New) The circuit of claim 37 wherein the circuitry for applying the second voltage to at least some of the first set of disabling lines and the circuitry for applying the first voltage to at least some of the second set of disabling lines are external to the information-storage circuit.

44. (New) The circuit of claim 32 wherein the sensing circuitry is configured to sense current when an information-defining nonlinear element is not present at the storage location of the selected first-set address line and a selected second-set conductive address line.

45. (New) The circuit of claim 44 wherein the sensing circuitry comprises an output line connected to each of the first set of address lines by a sensing nonlinear element.

46. (New) The circuit of claim 45 wherein the address circuitry comprises a first set of selectable disabling lines fewer in number than and connected to the first set of address lines by a first pattern of nonlinear elements, and circuitry for applying a second voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of address lines, the information-storage circuit further comprising additional address circuitry which itself comprises (i) a second set of selectable disabling lines fewer in number than and connected to the second set of address lines by a second pattern of nonlinear elements, and (ii) circuitry for applying a first voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of address lines, all of the nonlinear elements having a threshold activation voltage associated therewith, application of the threshold activation voltage across the nonlinear elements allowing current to flow therethrough.

47. (New) The circuit of claim 46 wherein all of the nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop, the output line being set to a fifth voltage such that current through a sensing rectifier will not flow if connected to a disabled address line of the first set of address lines.

48. (New) The circuit of claim 47 further comprising driver circuitry for setting the fifth voltage and amplifying the current sensed when an information-defining nonlinear element is not present at the storage location of the first and second address lines.

49. (New) The circuit of claim 44 further comprising driver circuitry for amplifying the current sensed when an information-defining nonlinear element is not present at the storage location of the first and second address lines.

50. (New) The circuit of claim 49 wherein the driver circuitry is external to the information-storage circuit.

51. (New) The circuit of claim 31 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

52. (New) The circuit of claim 51 wherein the first and second series of voltage drop elements are resistors.

53. (New) The circuit of claim 51 wherein the first and second series of voltage drop elements are nonlinear elements.

54. (New) The circuit of claim 53 wherein the nonlinear elements are rectifiers.

55. (New) The circuit of claim 54 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

56. (New) The circuit of claim 51 wherein the second voltage is ground or near to ground.

57. (New) The circuit of claim 32 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

58. (New) The circuit of claim 57 wherein the first and second series of voltage drop elements are resistors.

59. (New) The circuit of claim 57 wherein the first and second series of voltage drop elements are nonlinear elements.

60. (New) The circuit of claim 59 wherein the nonlinear elements are rectifiers.

61. (New) The circuit of claim 61 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

62. (New) The circuit of claim 57 wherein the second voltage is ground or near to ground.

63. (New) The circuit of claim 46 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

64. (New) The circuit of claim 63 wherein the first and second series of voltage drop elements are resistors.

65. (New) The circuit of claim 63 wherein the first and second series of voltage drop elements are nonlinear elements.

66. (New) The circuit of claim 65 wherein the nonlinear elements are rectifiers.

67. (New) The circuit of claim 66 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

68. (New) The circuit of claim 63 wherein the second voltage is ground or near to ground.

69. (New) The circuit of claim 31 wherein the circuit operates as a random access memory.

70. (New) The circuit of claim 31 wherein the circuit operates as a read only memory.

71. (New) The circuit of claim 31 wherein the circuit operates as a one-time-programmable read only memory.

72. (New) The circuit of claim 31 further comprising:

a. third and fourth sets of conductive address lines overlapping with each other and defining storage locations at overlap regions;

b. a second series of information-defining nonlinear elements bridging the address lines at least at some of the overlap regions, presence or absence of a nonlinear element at a storage location defining a bit state at the location,

the address circuitry being configured to also disable all but a selected one of the third set of address lines.

73. (New) The circuit of claim 72 further comprising additional sensing circuitry for sensing the presence or absence of a nonlinear information-defining element bridging the selected third-set

address line and at least a selected one of the fourth set of address lines to thereby determine the bit state at each storage location defined by selected address lines.

74. (New) The circuit of claim 31 wherein each storage location is a pixel of a display device.

75. (New) The circuit of claim 74 wherein the nonlinear elements are light emitting.

76. (New) The circuit of claim 74 wherein the nonlinear elements are light emitting diode.

77. (New) A method of storing and retrieving information, the method comprising the steps of:

a. providing first and second sets of conductive address lines overlapping with each other and defining storage locations at overlap regions;
b. storing information by bridging the address lines at least at some of the overlap regions with information-defining nonlinear elements, presence or absence of an information-defining nonlinear element at a storage location defining a bit state at the location;
c. disabling all but a selected one of the first set of address lines; and
d. reading the stored information by sensing the presence or absence of an information-defining nonlinear element bridging the selected first-set address line and a selected one of the second set of address lines to thereby determine the bit state at the storage location defined by the selected address lines.

78. (New) The method of claim 77 wherein the all but one of the first set of address lines is disabled by shifting a voltage thereon.

79. (New) The method of claim 77 further comprising the step of disabling all but a selected one of the second set of address lines.

80. (New) The method of claim 79 wherein the all but one of the second set of address lines is disabled by shifting a voltage thereon.

81. (New) The method of claim 80 wherein the information-defining nonlinear elements have a threshold activation voltage associated therewith, and further comprising the step of setting all but the selected one of the first set of address lines to a first voltage level and setting all but the selected one of the second set of address lines to a second voltage level, the first and second voltage levels differing by at least the threshold activation voltage.

82. (New) The method of claim 81 wherein the information-defining nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop so that an information-defining rectifier, if present at the storage location defined by the selected address lines, is forward biased.

83. (New) The method of claim 82 wherein the second voltage is ground or near to ground.

84. (New) The method of claim 77 wherein the reading step comprises sensing current when an information-defining nonlinear element is not present at the storage location of the selected first-set address line and a selected second-set conductive address line.

85. (New) The method of claim 77 further comprising the step of randomly rewriting the stored information.

86. (New) The method of claim 77 wherein the stored information cannot be rewritten.

87. (New) The method of claim 77 wherein the stored information is randomly writeable once.

STATEMENT OF STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES UNDER 37 C.F.R. §1.173(c)

Claim 1 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 2 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 3 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 4 (pending)

This claim was amended to change the dependency from cancelled claim 1 to newly filed independent claim 31. Support for the "sets of conductive address lines" language can be found throughout the specification, such as at column 1, lines 36-37 and column 3, lines 34-35.

Claim 5 (pending)

This claim was amended to change the dependency from cancelled claim 1 to newly filed independent claim 31. Support for this claim amendment can be found as delineated for claim 4, above.

Claim 6 (pending)

This claim was amended to change the dependency from cancelled claim 1 to newly filed independent claim 31. Support for the "circuitry" language can be found throughout the specification, such as at column 3, lines 54-55. Support for the "storage" language can be found throughout the specification, such as at column 7, lines 17-20.

Claim 7 (pending)

This claim was amended to change the dependency from cancelled claim 1 to newly filed independent claim 31. Support for the "circuitry" language can be found throughout the specification, such as at column 3, lines 54-55. Support for the "storage" language can be found throughout the specification, such as at column 7, lines 17-20.

Claim 8 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 1 to newly filed independent claim 31.

Claim 9 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 1 to newly filed independent claim 31.

Claim 10 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 1 to newly filed independent claim 31.

Claim 11 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 1 to newly filed independent claim 31.

Claim 12 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 1 to newly filed independent claim 31.

Claim 13 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 1 to newly filed independent claim 31.

Claim 14 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 15 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 16 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 17 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 18 (pending)

This claim is amended to place it in proper form as required and to change the

dependency from cancelled claim 17 to amended claim 5. Support for the "nonlinear elements" language can be found as delineated in claim 31, below.

Claim 19 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 17 to amended claim 5. Support for the "nonlinear elements" language can be found as delineated in claim 31, below.

Claim 20 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 21 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 14 to newly filed independent claim 31. Support for the "nonlinear elements" language can be found as delineated in claim 31, below.

Claim 22 (pending)

This claim is amended to place it in proper form as required and to change the dependency from cancelled claim 14 to amended claim 31.

Claim 23 (pending)

This claim is amended to place it in proper form as required.

Claim 24 (pending)

This claim is amended to place it in proper form as required.

Claim 25 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 26 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 27 (cancelled)

This claim is cancelled because it is a duplicate of a claim in the parent application.

Claim 28 (pending)

Claim 29 (pending)

Claim 30 (pending)

Claim 31 (pending)

Support for this claim can be found throughout the specification, such as at Figures 3-5 and 12-14. Additional support can be found in column 7, lines 13-67, column 9, lines 39-42, column 11, lines 49-58 and column 15, lines 61-62.

Claim 32 (pending)

Support for the "sensing circuitry" language can be found throughout the specification, such as at column 7 lines 30-54.

Claim 33 (pending)

Support for the "disabling by shifting" language can be found throughout the specification, such as at column 17, lines 4-5, and column 7, lines 45-46.

Claim 34 (pending)

Support for the "additional address circuitry" language can be found in Figures 3-5 and 14, and additionally throughout the specification, such as at column 7, line 52, and column 9, lines 39-41.

Claim 35 (pending)

Support for this claim can be found as delineated for claim 33, above.

Claim 36 (pending)

Support for this claim can be found in figure 12 and throughout the specification as delineated in claim 31, above. Additional support can be found at column 7, lines 60-67 and column 8, lines 1-5.

Claim 37 (pending)

Support for this claim can be found in Figures 3-5, 13 and 14, and throughout the specification as delineated in claims 36 and 31, above. Additional support can be found at column 8, lines 5-9, column 9, lines 38-67 and column 10, lines 1-11.

Claim 38 (pending)

Support for this claim can be found throughout the specification, such as at column 7, lines 36-37.

Claim 39 (pending)

Support for this claim can be found as delineated in claim 36, above.

Claim 40 (pending)

Support for the "rectifier" language can be found throughout the specification, such as at column 6, lines 58-67.

Claim 41 (pending)

Support for the "rectifier" language can be found throughout the specification, such as at column 6, lines 58-67.

Claim 42 (pending)

Support for this claim can be found throughout the specification, such as at column 7, line 56.

Claim 43 (pending)

Support for this claim can be found in Figures 2, 3 and 6-11. Additional support can be found throughout the specification, such as at column 6, lines 12-15 and column 14, lines 5-8.

Claim 44 (pending)

Support for this claim can be found throughout the specification, such as at column 8, lines 48-54.

Claim 45 (pending)

Support for this claim can be found in Figures 3-5, and throughout the specification, such as at column 8, lines 30-49.

Claim 46 (pending)

Support for this claim can be found as delineated in claims 36 and 37, above.

Claim 47 (pending)

Support for this claim can be found as delineated in claim 41, above, and throughout the specification, such as at column 8, lines 30-32.

Claim 48 (pending)

Support for this claim can be found in Figures 4-5 and throughout the specification, such as at column 10, lines 12-30.

Claim 49 (pending)

Support for this claim can be found as delineated in claim 48, above.

Claim 50 (pending)

Support for this claim can be found in Figures 3, 13, and 14.

Claim 51 (pending)

Support for this claim can be found in Figures 3-5, 13, and 14. Additionally, support can be found throughout the specification, such as at column 7, lines 24-29.

Claim 52 (pending)

Support for this claim can be found in Figures 3-5 and 14. Additionally, support can be found throughout the specification, such as at column 7, lines 24-26.

Claim 53 (pending)

Support for this claim can be found in figure 13, and throughout the specification such as at column 7, lines 24-29 and column 12, lines 15-24.

Claim 54 (pending)

Support for this claim can be found as delineated in claim 53, above.

Claim 55 (pending)

Support for this claim can be found throughout the specification, such as at column 7, line 56.

Claim 56 (pending)

Support for this claim can be found throughout the specification, such as at column 12, lines 18-20.

Claim 57 (pending)

Support for this claim can be found as delineated in claim 51, above.

Claim 58 (pending)

Support for this claim can be found as delineated in claim 52, above.

Claim 59 (pending)

Support for this claim can be found as delineated in claim 53, above.

Claim 60 (pending)

Support for this claim can be found as delineated in claim 54, above.

Claim 61 (pending)

Support for this claim can be found as delineated in claim 55, above.

Claim 62 (pending)

Support for this claim can be found as delineated in claim 56, above.

Claim 63 (pending)

Support for this claim can be found as delineated in claim 51, above.

Claim 64 (pending)

Support for this claim can be found as delineated in claim 52, above.

Claim 65 (pending)

Support for this claim can be found as delineated in claim 53, above.

Claim 66 (pending)

Support for this claim can be found as delineated in claim 54, above.

Claim 67 (pending)

Support for this claim can be found as delineated in claim 55, above.

Claim 68 (pending)

Support for this claim can be found as delineated in claim 56, above.

Claim 69 (pending)

Support for this claim can be found throughout the specification, such as at column 11, line 67 and column 12, lines 1 and 2.

Claim 70 (pending)

Support for this claim can be found throughout the specification, such as at column 3, lines 29-31.

Claim 71 (pending)

Support for this claim can be found throughout the specification, such as at column 11, lines 63-66.

Claim 72 (pending)

Support for this claim can be found throughout the specification, such as at column 10, lines 57-65.

Claim 73 (pending)

Support for this claim can be found as delineated in claim 34, above.

Claim 74 (pending)

Support for this claim can be found throughout the specification, such as at column 15, lines 61-67.

Claim 75 (pending)

Support for this claim can be found as delineated in claim 74, above.

Claim 76 (pending)

Support for this claim can be found as delineated in claim 74, above.

Claim 77 (pending)

Support for this claim can be found as delineated in claims 31 and 32, above.

Claim 78 (pending)

Support for this claim can be found as delineated in claim 33, above.

Claim 79 (pending)

Support for this claim can be found as delineated in claim 34, above.

Claim 80 (pending)

Support for this claim can be found as delineated in claim 35, above.

Claim 81 (pending)

Support for this claim can be found as delineated in claim 36, above.

Claim 82 (pending)

Support for this claim can be found as delineated in claim 40, above.

Claim 83 (pending)

Support for this claim can be found as delineated in claim 42, above.

Claim 84 (pending)

Support for this claim can be found as delineated in claim 44, above.

Claim 85 (pending)

Support for this claim can be found as delineated in claim 69, above.

Claim 86 (pending)

Support for this claim can be found as delineated in claim 70 above.

Claim 87 (pending)

Support for this claim can be found as delineated in claim 71, above.

REMARKS

This Preliminary Amendment is being submitted to cancel 1-3 14-17, 20, and 25-27 because they are duplicates of claims that issued in the parent to this patent, namely, U.S. Patent No. 5,673,218. Claims 31-87 have been added to broaden the scope of the claimed subject matter. Upon entry of the present amendment, claims 4-13, 18, 19, 21-24, and 28-87 will be pending.

Applicant respectfully requests entry of this Preliminary Amendment prior to examination of the application on the merits. Further, Applicant respectfully submits that no new matter is added by the Preliminary Amendment.

Respectfully submitted,

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CLEAN COPY OF ALL PENDING CLAIMS FOLLOWING ENTRY OF THE AMENDMENT

4. The circuit of claim 31, wherein one of the sets of conductive address lines is a plurality of generally parallel doped regions within a semiconductor material.

5. The circuit of claim 31, wherein one of the sets of conductive address lines is a plurality of generally parallel metalized regions.

6. The circuit of claim 31, wherein said addressing circuitry comprises circuitry to sequentially select storage locations.

7. The circuit of claim 31, wherein said addressing circuitry comprises circuitry to randomly select storage locations.

8. The circuit of claim 31, further comprising display means for displaying alphanumeric or graphic information to a user.

9. The circuit of claim 31, further comprising input means to enable its user to alter its operation.

10. The circuit of claim 31, wherein part or all of said circuit is removable or replaceable.

11. The circuit of claim 31, wherein output from the circuit is in a digital format.

12. The circuit of claim 31, wherein output from the circuit is in an analog format.

13. The circuit of claim 31, wherein output from the circuit is in either a digital format or an analog format.

18. The circuit of claim 5, wherein said nonlinear elements are of the metal-on-semiconductor junction type.

19. The circuit of claim 5, wherein said nonlinear elements are of the p-n junction type.

21. The circuit of claim 31, wherein said nonlinear elements are comprised by a transistor as the base-emitter junction.

22. The circuit of claim 31, further comprising means for retaining the address of the information to be accessed.

23. The circuit of claim 22, further comprising means for incrementing the retained address.

24. The circuit of claim 22, further comprising means for setting the retained address.

28. An electronic array of selectable points comprising:

a plurality of conductive means;

a second plurality of conductive means;

a plurality of selectable points where a point of said plurality of selectable points is present in the general vicinity of each point of intersection of each conductive means of the first said plurality of conductive means and each conductive means of the second said plurality of conductive means;

means for selecting a conductive means of one plurality of conductive means, and means for biasing the conductive means of the other plurality of conductive means such that each said selectable point present between a conductive means of said biased plurality of conductive means and a conductive means of the other said plurality of conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of conductive means by shifting the voltage of those biased conductive means that are to be disabled.

29. The electronic array of selectable points of claim 28, wherein said means for selecting a conductive means of one plurality of generally parallel conductive means comprises:

means for biasing the conductive means of the said one plurality of conductive means such that each said selectable point present between a conductive means of said biased plurality of conductive means and a conductive means of the other said plurality of conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of conductive means by shifting the voltage of those biased conductive means that are to be disabled.

30. The electronic array of selectable points of claim 28, wherein said each selectable point comprises a light emitting diode (LED) which will emit light when forward biased.

31. An information-storage circuit, the circuit comprising:

a. first and second sets of conductive address lines overlapping with each other and defining storage locations at overlap regions;

b. a series of information-defining nonlinear elements bridging the address lines at least at some of the overlap regions, presence or absence of a nonlinear element at a storage location defining a bit state at the location; and

c. address circuitry for disabling all but a selected one of the first set of address lines.

32. The circuit of claim 31 further comprising sensing circuitry for sensing the presence or absence of a nonlinear information-defining element bridging the selected first-set address line and at least a selected one of the second set of address lines to thereby determine the bit state at each storage location defined by selected address lines.

33. The circuit of claim 31 wherein the all but one of the first set of address lines is disabled by shifting a voltage thereon.

34. The circuit of claim 31 further comprising additional address circuitry for disabling all but a selected one of the second set of address lines.

35. The circuit of claim 34 wherein the all but one of the second set of address lines is disabled by shifting a voltage thereon.

36. The circuit of claim 34 wherein:

a. the information-defining nonlinear elements have a threshold activation voltage associated therewith;

b. the address circuitry comprises circuitry for setting all but the selected one of the first set of address lines to a first voltage level; and

c. the additional address circuitry comprises circuitry for setting all but the selected one of the second set of address lines to a second voltage level, the first and second voltage levels differing by at least the threshold activation voltage.

37. The circuit of claim 36 wherein:

a. the address circuitry further comprises a first set of selectable disabling lines fewer in number than and connected to the first set of address lines by a first pattern of nonlinear elements, and circuitry for applying a third voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of address lines; and

b. the additional address circuitry further comprises a second set of selectable disabling lines fewer in number than and connected to the second set of address lines by a second pattern

of nonlinear elements, and circuitry for applying a fourth voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of address lines.

38. The circuit of claim 37 wherein the third voltage is substantially equal to the second voltage and the fourth voltage is substantially equal to the first voltage.

39. The circuit of claim 38 wherein all of the nonlinear elements have a threshold activation voltage associated therewith, application of the threshold activation voltage across the nonlinear elements allowing current to flow therethrough.

40. The circuit of claim 36 wherein the information-defining nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop so that an information-defining rectifier, if present at the storage location defined by the selected address lines, is forward biased.

41. The circuit of claim 39 wherein all of the nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop.

42. The circuit of claim 36 wherein the second voltage is ground or near to ground.

43. The circuit of claim 37 wherein the circuitry for applying the second voltage to at least some of the first set of disabling lines and the circuitry for applying the first voltage to at least some of the second set of disabling lines are external to the information-storage circuit.

44. The circuit of claim 32 wherein the sensing circuitry is configured to sense current when an information-defining nonlinear element is not present at the storage location of the selected first-set address line and a selected second-set conductive address line.

45. The circuit of claim 44 wherein the sensing circuitry comprises an output line connected to each of the first set of address lines by a sensing nonlinear element.

46. The circuit of claim 45 wherein the address circuitry comprises a first set of selectable disabling lines fewer in number than and connected to the first set of address lines by a first pattern of nonlinear elements, and circuitry for applying a second voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of address lines, the

information-storage circuit further comprising additional address circuitry which itself comprises (i) a second set of selectable disabling lines fewer in number than and connected to the second set of address lines by a second pattern of nonlinear elements, and (ii) circuitry for applying a first voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of address lines, all of the nonlinear elements having a threshold activation voltage associated therewith, application of the threshold activation voltage across the nonlinear elements allowing current to flow therethrough.

47. The circuit of claim 46 wherein all of the nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop, the output line being set to a fifth voltage such that current through a sensing rectifier will not flow if connected to a disabled address line of the first set of address lines.

48. The circuit of claim 47 further comprising driver circuitry for setting the fifth voltage and amplifying the current sensed when an information-defining nonlinear element is not present at the storage location of the first and second address lines.

49. The circuit of claim 44 further comprising driver circuitry for amplifying the current sensed when an information-defining nonlinear element is not present at the storage location of the first and second address lines.

50. The circuit of claim 49 wherein the driver circuitry is external to the information-storage circuit.

51. The circuit of claim 31 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

52. The circuit of claim 51 wherein the first and second series of voltage drop elements are resistors.

53. The circuit of claim 51 wherein the first and second series of voltage drop elements are nonlinear elements.

54. The circuit of claim 53 wherein the nonlinear elements are rectifiers.

55. The circuit of claim 54 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

56. The circuit of claim 51 wherein the second voltage is ground or near to ground.

57. The circuit of claim 32 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

58. The circuit of claim 57 wherein the first and second series of voltage drop elements are resistors.

59. The circuit of claim 57 wherein the first and second series of voltage drop elements are nonlinear elements.

60. The circuit of claim 59 wherein the nonlinear elements are rectifiers.

61. The circuit of claim 61 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

62. The circuit of claim 57 wherein the second voltage is ground or near to ground.

63. The circuit of claim 46 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

64. The circuit of claim 63 wherein the first and second series of voltage drop elements are resistors.

65. The circuit of claim 63 wherein the first and second series of voltage drop elements are nonlinear elements.

66. The circuit of claim 65 wherein the nonlinear elements are rectifiers.

67. The circuit of claim 66 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

68. The circuit of claim 63 wherein the second voltage is ground or near to ground.

69. The circuit of claim 31 wherein the circuit operates as a random access memory.

70. The circuit of claim 31 wherein the circuit operates as a read only memory.

71. The circuit of claim 31 wherein the circuit operates as a one-time-programmable read only memory.

72. The circuit of claim 31 further comprising:

a. third and fourth sets of conductive address lines overlapping with each other and defining storage locations at overlap regions;

b. a second series of information-defining nonlinear elements bridging the address lines at least at some of the overlap regions, presence or absence of a nonlinear element at a storage location defining a bit state at the location,

the address circuitry being configured to also disable all but a selected one of the third set of address lines.

73. The circuit of claim 72 further comprising additional sensing circuitry for sensing the presence or absence of a nonlinear information-defining element bridging the selected third-set address line and at least a selected one of the fourth set of address lines to thereby determine the bit state at each storage location defined by selected address lines.

74. The circuit of claim 31 wherein each storage location is a pixel of a display device.

75. The circuit of claim 74 wherein the nonlinear elements are light emitting.

76. The circuit of claim 74 wherein the nonlinear elements are light emitting diode.

77. A method of storing and retrieving information, the method comprising the steps of:

a. providing first and second sets of conductive address lines overlapping with each other and defining storage locations at overlap regions;

b. storing information by bridging the address lines at least at some of the overlap regions with information-defining nonlinear elements, presence or absence of an information-defining nonlinear element at a storage location defining a bit state at the location;

c. disabling all but a selected one of the first set of address lines; and

d. reading the stored information by sensing the presence or absence of an information-defining nonlinear element bridging the selected first-set address line and a selected one

of the second set of address lines to thereby determine the bit state at the storage location defined by the selected address lines.

78. The method of claim 77 wherein the all but one of the first set of address lines is disabled by shifting a voltage thereon.

79. The method of claim 77 further comprising the step of disabling all but a selected one of the second set of address lines.

80. The method of claim 79 wherein the all but one of the second set of address lines is disabled by shifting a voltage thereon.

81. The method of claim 80 wherein the information-defining nonlinear elements have a threshold activation voltage associated therewith, and further comprising the step of setting all but the selected one of the first set of address lines to a first voltage level and setting all but the selected one of the second set of address lines to a second voltage level, the first and second voltage levels differing by at least the threshold activation voltage.

82. The method of claim 81 wherein the information-defining nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop so that an information-defining rectifier, if present at the storage location defined by the selected address lines, is forward biased.

83. The method of claim 82 wherein the second voltage is ground or near to ground.

84. The method of claim 77 wherein the reading step comprises sensing current when an information-defining nonlinear element is not present at the storage location of the selected first-set address line and a selected second-set conductive address line.

85. The method of claim 77 further comprising the step of randomly rewriting the stored information.

86. The method of claim 77 wherein the stored information cannot be rewritten.

87. The method of claim 77 wherein the stored information is randomly writeable once.